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Protection System Design and Application Considerations for Advanced Line Differential Relaying

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1 INTRODUCTION

As a unit protection, the differential protection principle is considered superior with respect to selectivity, sensitivity, and speed of operation as compared with directional comparison, phase comparison, or stepped distance schemes.

The differential function responds to the sum of all the currents of its zone of protection. Ideally, this sum equals zero under all events except for internal faults. Practically, measurement errors and shunt elements inside the zone may create a spurious differential signal.

The key benefits of differential protection include good performance on multiterminal and series-compensated lines and lines of any length as compared with distance or directional comparison schemes. Microprocessor technology has made new functions possible, including better security against current transformer (CT) saturation, line-charging current compensation, and accommodating in-line transformers.

This paper describes an optimized line current differential scheme working with limited bandwidth channels, while providing for high speed, sensitivity, and security under CT saturation.

2 TYPICAL LINE CURRENT DIFFERENTIAL SYSTEM

The most distinctive feature of a line current differential protection system is that it consists of multiple relays operating independently and linked by a digital communications channel (Fig. 1).

Each relay samples its analog input currents via an analog-to-digital (A/D) converter to obtain a digital representation (i_D) of the analog inputs (i_A).

The sampling may be performed at a constant rate or at a variable rate, tracking the power system frequency. The samples may be taken asynchronously with the local relay time or synchronously with the absolute time to simplify implementation of synchrophasor measurements.

Channels traditionally used for line current differential protection are limited in bandwidth (64 kbps is a typical value), and therefore only limited amounts of data can be exchanged between the relays. Some relays exchange samples of currents, some relays work on phasors, and yet others work on nonconventional quantities such as a positive or negative current charge between consecutive zero crossings of the current.

This variety of approaches is driven by the substantial design challenge of conveying sufficient amounts of data to facilitate adequate protection performance, meeting channel bandwidth limitations, and providing for robust data synchronization, all at the same time.

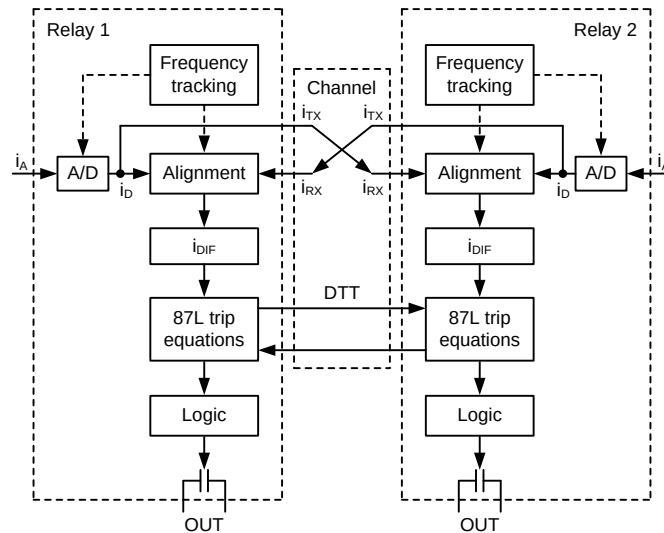


Fig. 1: Simplified architecture of a typical line current differential system

Until now, the Global Positioning System (GPS) has been the only practical way to provide for common timing across wide areas. Reliance on a satellite system and additional devices is not an ideal protection solution. Terrestrial systems are emerging for providing a common time reference [1]. These systems are synchronized to GPS—for the benefit of using true time under normal conditions—via multiple receivers located at multiple geographical locations. They continue to provide common timing should all the GPS inputs be lost. These systems are a part of the communications used for the relay; therefore, they are a safe means of providing for external time reference without introducing more devices, unnecessary interdependencies, or reduced reliability or availability.

3 RELAY DESIGN CONSTRAINTS BECAUSE OF AVAILABLE CHANNEL BANDWIDTH

To realize the amount of data that can be conveyed for protection purposes over a 64 kbps channel, let us assume a sampling rate of 16 samples per cycle and review the following: 64,000 bits per second = 1,067 bits per a 60 Hz power cycle = 267 bits per quarter of a 60 Hz power cycle.

As with any digital communications scheme, there is always certain overhead in the communications packet on top of the actual payload:

- A header is required for packet identification. A total of 15 bits may be needed.
- The integrity of the data must be protected by redundancy checks. A total of 32 bits is typically needed.
- Channel-based synchronization methods need to append certain time values to the packet. A total of 16 bits or more may be required.
- The packet must support basic addressing. A total of 4 to 8 bits may be required.
- Direct transfer tripping (DTT) and other flags must be supported. A total of 4 to 8 bits may be used for this purpose.

The above adds 50 to 80 bits of overhead.

It is clear that the protection-driven payload and the communications-driven constraints must be addressed in a design to yield a high-performance scheme. It is important to select which quantities are sent, how often, and how they are encoded, packetized, and protected for integrity. Consider the packet (content described in Table 1) and protection equations presented in this paper. This solution works with 1 kHz samples of currents and utilizes proven Alpha Plane protection equations [2].

The payload of Table 1 can be encoded using slightly more than 100 bits, allowing us to send packets every 3 milliseconds (3 milliseconds at 64 kbps allows 192 bits).

The instantaneous values are total line currents at the sending terminal (a sum of all the local currents, such as from the two breakers of a dual-breaker termination), while the restraint terms are sums of magnitudes of all the local currents (such as from the two breakers of a dual-breaker termination).

Symbol	Meaning
$i_{A(k)}$	Present (k-th) sample of the line current, A-phase
$i_{A(k-1)}$	k-1 sample of the line current, A-phase
$i_{A(k-2)}$	k-2 sample of the line current, A-phase
$i_{B(k)}$	As above, B-phase
$i_{B(k-1)}$	
$i_{B(k-2)}$	
$i_{C(k)}$	As above, C-phase
$i_{C(k-1)}$	
$i_{C(k-2)}$	
I_{AR}	Restraint term, A-phase
I_{BR}	Restraint term, B-phase
I_{CR}	Restraint term, C-phase
I_{QR}	Negative-sequence restraint term
I_{GR}	Zero-sequence (3I0) restraint term

Table 1: Packet Payload Definition

The selected payload provides the following benefits:

- Fresh data are sent every 3 milliseconds, or more than five times a 60 Hz cycle, minimizing latencies and speeding up operation of the relay.
- A packet lost just before or during an internal fault erases only 3 milliseconds of data, allowing for fast recovery and preventing delayed operation of the relay.
- Working with 1 kHz samples offers good fidelity of differential current measurements and allows the calculating of harmonics for in-line transformer applications and fast detection of saturated CTs.
- Sending three samples of instantaneous current per packet improves the payload-to-overhead ratio.
- Sending one value of a restraint per packet (or per three samples of instantaneous values) reduces bandwidth requirements, while it is sufficient for protection applications.
- Restraint quantities are magnitudes that can be encoded using fewer bits.
- The packet format makes the solution scalable, because it works with any number of local currents at a given line terminal. The packet always contains the partial differential and partial restraint terms.

4 DUAL-BREAKER TERMINALS AND PROTECTION SECURITY

Dual-breaker applications working with breaker currents may create some protection challenges. Consider the three-terminal line configuration of Fig. 2, with each line end terminated as a dual-breaker connection.

In the proposed design, each relay calculates its partial differential and partial restraint term as follows: $i_{A(T1)} = i_{1A} + i_{2A}$ and $I_{AR(T1)} = I_{1A} + I_{2A}$ (B- and C-phases are similar) and $I_{QR(T1)} = I_{1Q} + I_{2Q}$ and $I_{GR(T1)} = I_{1G} + I_{2G}$, where lowercase symbols are instantaneous values and uppercase symbols are magnitudes. Similar terms are calculated for Terminals T2 and T3.

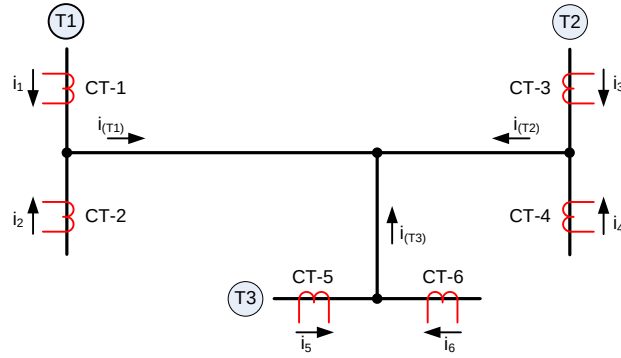


Fig. 2: Sample three-terminal, dual-breaker line configuration

The above quantities constitute the core protection payload per Table 1. Each terminal calculates its partial terms and sends them to its peers.

If an external fault occurs at the T1 terminal, under CT saturation, the partial differential current sent by this terminal may have a considerable error in it. However, at the same time, this terminal sends a restraint term that reflects the external fault current, feeding the Alpha Plane trip equations with information to counterbalance the errors in the differential signal.

Upon receiving and aligning all the partial terms, each relay calculates the total line differential and restraint currents for the 87LP (phase) function (A-phase is shown; B- and C-phases are similar):

$$i_{ADIF} = i_{A(T1)} + i_{A(T2)} + i_{A(T3)} = i_{1A} + i_{2A} + i_{3A} + i_{4A} + i_{5A} + i_{6A}$$

$$I_{ARST} = I_{AR(T1)} + I_{AR(T2)} + I_{AR(T3)} = I_{1A} + I_{2A} + I_{3A} + I_{4A} + I_{5A} + I_{6A}$$

and for the 87LQ (negative-sequence) and 87LG (ground) functions:

$$I_{QRST} = I_{QR(T1)} + I_{QR(T2)} + I_{QR(T3)} = I_{1Q} + I_{2Q} + I_{3Q} + I_{4Q} + I_{5Q} + I_{6Q}$$

$$I_{GRST} = I_{GR(T1)} + I_{GR(T2)} + I_{GR(T3)} = I_{1G} + I_{2G} + I_{3G} + I_{4G} + I_{5G} + I_{6G}$$

In this way, each relay in the line current differential system derives the true value of the restraint current, regardless of fault location or short-circuit capacity behind any given relay.

In addition to natural levels of restraint, the relay incorporates external fault detection (EFD) logic to increase security during external faults and relax the CT requirements.

Fig. 3 presents the logic. This method is successfully used in bus and transformer differential relays [3] [4]. An increase in the instantaneous restraining signal (above the threshold P) without a similar increase in the differential current (multiplier q) signifies an external fault.

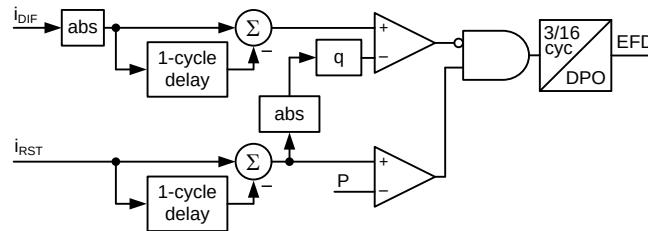


Fig. 3: External fault detection logic

Each terminal derives its own instantaneous restraining current based on its local currents and the partial differential terms from the remote terminals (refer to Fig. 2, the phase index—A, B, or C—is omitted): $i_{RST(T1)} = |i_1| + |i_2| + |i_{(T2)}| + |i_{(T3)}|$ and $i_{RST(T2)} = |i_3| + |i_4| + |i_{(T1)}| + |i_{(T3)}|$ and $i_{RST(T3)} = |i_5| + |i_6| + |i_{(T1)}| + |i_{(T2)}|$, where $|x|$ stands for the absolute value of an instantaneous signal x .

The above terms are used locally. Each relay executes the logic using its instantaneous local restraint and the line differential current. The relay at the terminal with an external fault detects it from the through-fault current. The other relays may or may not detect the fault, depending on the current

flow. Therefore, the EFD flag derived locally is added to the communications payload. All of the relays work with the same amount of information, and all behave correctly.

5 GENERALIZED ALPHA PLANE FOR MULTITERMINAL APPLICATIONS

The Alpha Plane current differential principle compares individual magnitudes and angles of the zone currents. The principle is easy to understand for the case of a two-terminal line. Under balanced conditions, the two currents of the zone (I_L and I_R) are equal in magnitude and opposite in phase. This yields an operating point on the Alpha Plane of $k = 1 \angle 180^\circ$. Under internal faults, the complex current ratio, k , departs from this ideal blocking point, allowing the relay to operate. Blocking and operating regions are shaped as pictured in Fig. 4 with two easy-to-set parameters, restraint radius and angle.

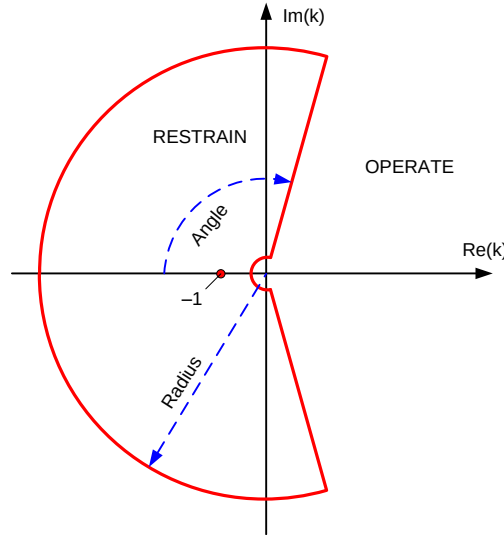


Fig. 4: Typical Alpha Plane characteristic

87LP, 87LQ, and/or 87LG Alpha Plane elements are applied. This principle has been successfully implemented and proven by a long field record [5]. The most important advantages are significant tolerance to CT saturation and synchronization errors, excellent sensitivity and speed of the 87LQ and 87LG elements, significant tolerance of the 87LQ and 87LG elements to the line-charging current, and good performance in series-compensated lines.

The N-terminal Alpha Plane concept calculates a two-terminal equivalent for a general N-terminal case and applies the tried-and-true Alpha Plane principle to the two equivalent currents.

6 LINE-CHARGING CURRENT COMPENSATION

Line-charging current affects both the security and dependability of differential protection.

Line-charging compensation removes the charging current from the differential current.

The line capacitance (Fig. 5) can be represented by a lumped parameter model at each terminal of the line that allows the line current differential relay to measure the voltage.

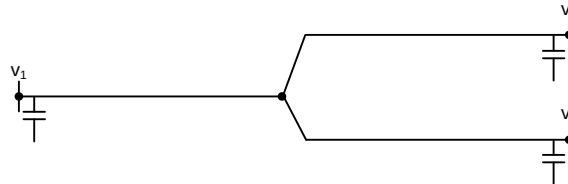


Fig. 5: Lumped parameter three-terminal line

$$i_{C_TOTAL} = C_{TOTAL} \cdot \frac{d}{dt} v_{AVERAGE}$$

The average line voltage can be approximated by the average terminal voltage, and therefore:

$$i_{C_TOTAL} = C_{TOTAL} \cdot \frac{1}{3} \cdot \frac{d}{dt} (v_1 + v_2 + v_3)$$

In other words, the total charging current is the sum of three components, each derived from a single line terminal voltage: $i_{C1} = \frac{1}{3} \cdot C_{TOTAL} \cdot \frac{d}{dt} v_1$ and $i_{C2} = \frac{1}{3} \cdot C_{TOTAL} \cdot \frac{d}{dt} v_2$ and $i_{C3} = \frac{1}{3} \cdot C_{TOTAL} \cdot \frac{d}{dt} v_3$

Each terminal calculates a share of the total charging current based on local voltage and a portion of the total line capacitance proportional to the number of line terminals that perform the compensation at any given time. These fractions of the charging current, when summed up by the final differential current, will null out the actual charging current.

This principle is key—the line current differential system effectively calculates the charging current based on the average voltage from all line terminals, without sending any voltages between the relays. Instead, each terminal subtracts its share of the charging current from the measured current and sends it to its peers.

This scheme makes the charging current compensation feature more immune to problems with voltage transformers (VTs). In a way, individual relays in the line current differential system work as remote backup voltage sources for each other. If all voltages are lost, the relay automatically desensitizes to ensure security and continues working with currents only.

7 IN-LINE TRANSFORMERS

In some applications, a line and a transformer are installed without a breaker in between to separate the two pieces of equipment (see Fig. 6).

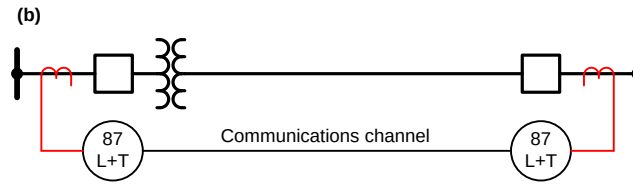


Fig. 6: Transformer and line protection

Being a differential principle, the Alpha Plane technique can provide short-circuit protection for power transformers. For a general case on an N-winding transformer, the differential and restraining signals are sums of ratio-matched and vector-compensated winding currents. This observation leads to a simple relay implementation of compensating the individual currents for transformer connections based on the position of the current with respect to the various transformer windings and running the regular line current differential communications and processing algorithms based on the transformer-compensated currents (Fig. 7).

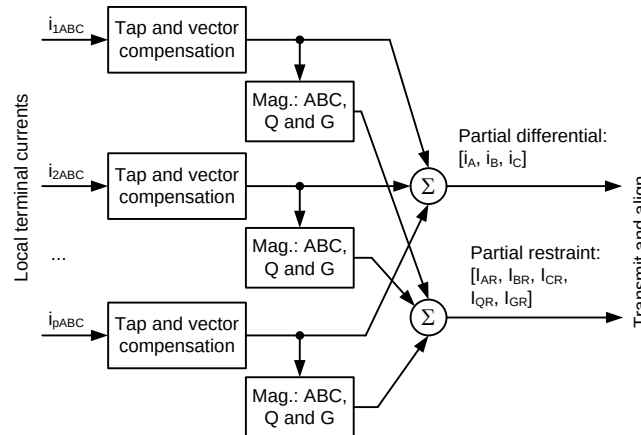


Fig. 7: Compensating currents for transforming connections in a line current differential scheme

Inrush and overexcitation harmonic blocking are naturally performed by measuring the second and fifth harmonics in the differential current and comparing them with user thresholds. Cross-phase blocking or the fourth harmonic can be used, depending on the design and user preferences [4] [6].

8 SPEED OF OPERATION

Internal relay data latencies, algorithm delay, and channel delay limit the operating speed of a line current differential relay. Direct fiber connections add negligible delay to the scheme. Multiplexed channels can add a delay in the range of a few milliseconds to tens of milliseconds, depending primarily on the number of devices passing the data between the relays.

Internal relay data latency includes collecting and passing samples from the A/D converter, processing the local data for transmission, assembling outgoing packets, accepting incoming packets, aligning the data, processing the global differential calculations, and asserting the outputs.

The algorithm time refers to the length of a data window that must be available before a trip decision can be made. It should not be mistaken for the length of the filter data windows—it is simply a point in time when enough information is available to make a reliable trip decision.

In this respect, the 87LQ and 87LG functions are very fast. Even when using full-cycle filters, these functions assert their outputs in a fraction of a cycle (see Fig. 8).

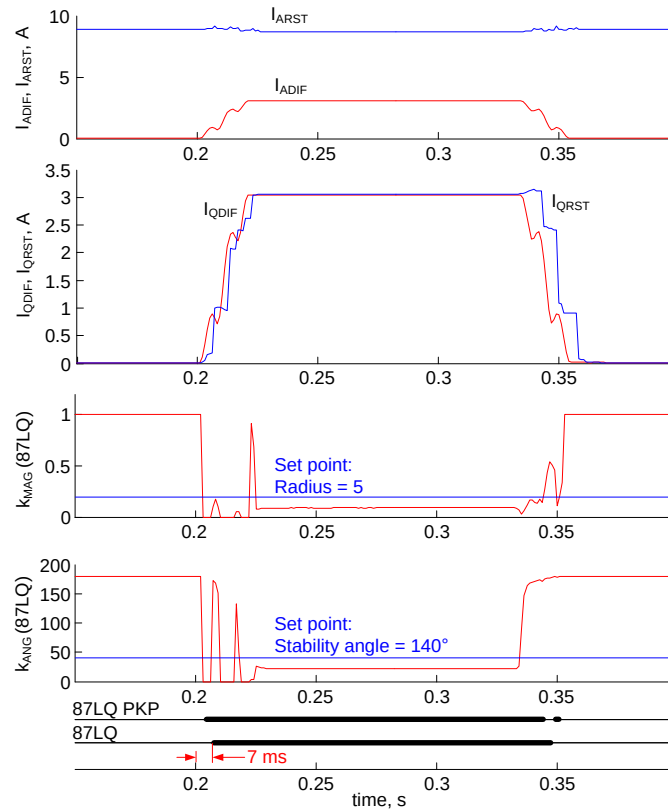


Fig. 8: Operation of the 87LQ function for a 100 Ω AG fault

This short response time is because they are not biased by the load current prior to the fault. Owing to the proper restraining techniques, the external fault detection logic, and the charging current compensation, these functions can be operated at their natural speed without introducing much intentional delay for security purposes.

In addition, the 87LP element uses a high-speed element in parallel with the full-cycle filtered path. The high-speed differential protection is feasible in the proposed scheme because the key signals are available as samples. In a differential scheme, most of the transients cancel in the operating signal, and therefore it is secure to make trip decisions based on less than a full cycle of data. CT saturation may cause problems, but this issue is addressed by fast and reliable EFD logic. If the EFD asserts, the high-speed path is inhibited.

As a result of careful design, the relay architecture minimizes data latencies. The applied protection algorithms are fast under internal fault conditions because they are restrained in a way that does not penalize speed. Overall, the presented solution provides for subcycle trip times if used with fast communications channels.

9 CONCLUSION

This paper outlines characteristics for a next generation line current differential scheme:

- Channel-based and external time reference-based synchronization methods produce a robust system for general application.
- A terrestrial, GPS-independent time source makes line current differential applications with asymmetrical channels safer and more dependable.
- Fallback strategies allow the system to ride through temporary loss of the timing source.
- The Alpha Plane restraining technique is used for optimum security. The size and structure of the communications payload are independent of the number of terminals or the number of local currents in the system.
- The system works with high-fidelity current information, allowing a fast external fault detection logic as well as harmonic measurements for in-line transformer applications.
- The combination of external fault detection and the proper restraining techniques makes the relay both very secure and fast.
- Line-charging current compensation is incorporated, enhancing security during line energization and improving sensitivity to internal faults.
- Communications packets and data handling internal to the relays were designed for low latencies. Combined with high-speed performance of the applied protection equations, this enables subcycle trip times in applications with fast communications channels.

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